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Managing high-voltage line ripple rejection using high bandwidth DC-DC

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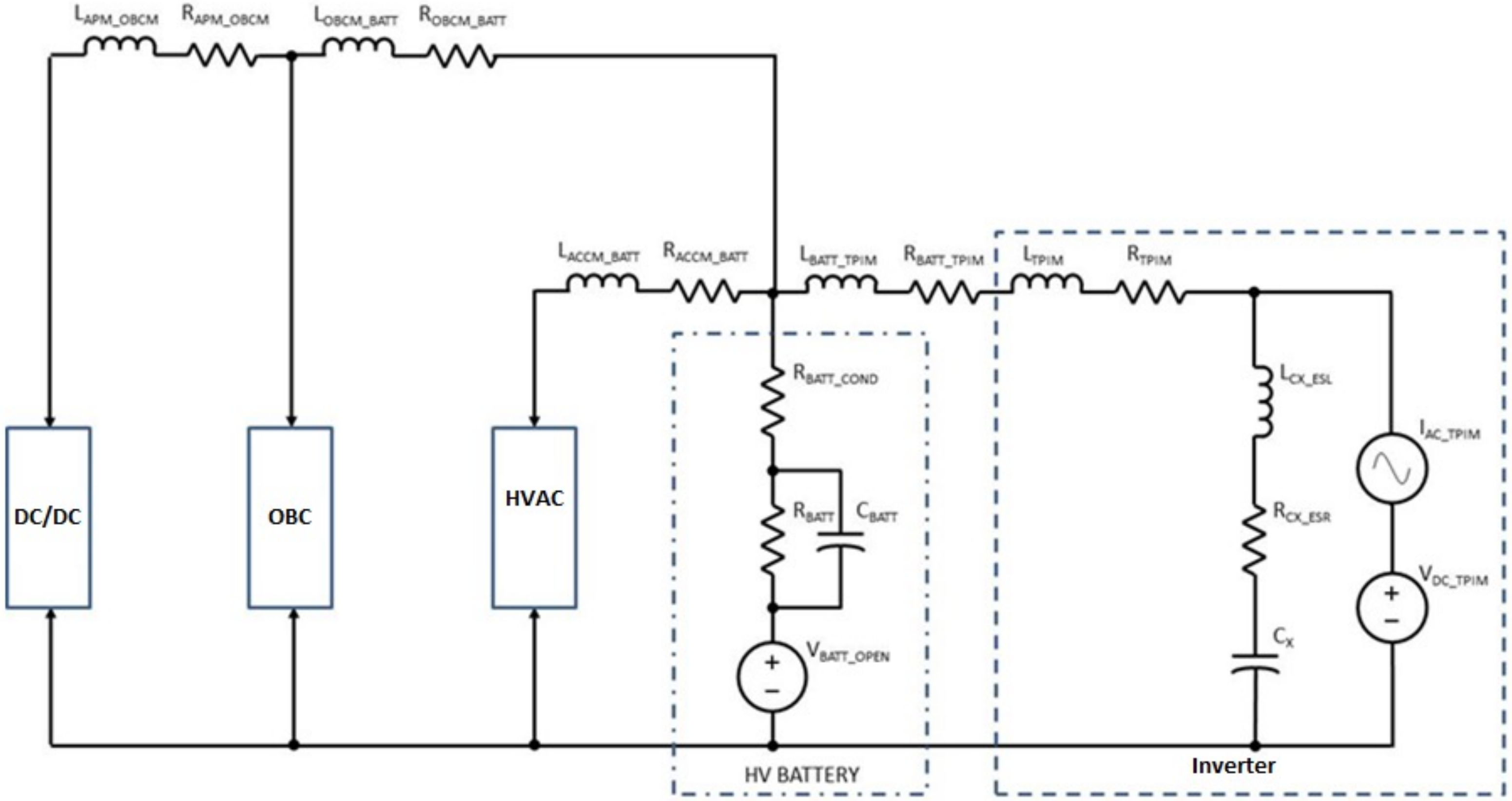
Electric vehicle HV bus overview and inverter ripple

High voltage ripple occurs on high voltage bus during propulsion and regeneration as a result of inverter's (PIM) operation

Most of the ripple is filtered by inverter's bulk capacitor but significant part is injected to HV bus and can cause issues for other power converters

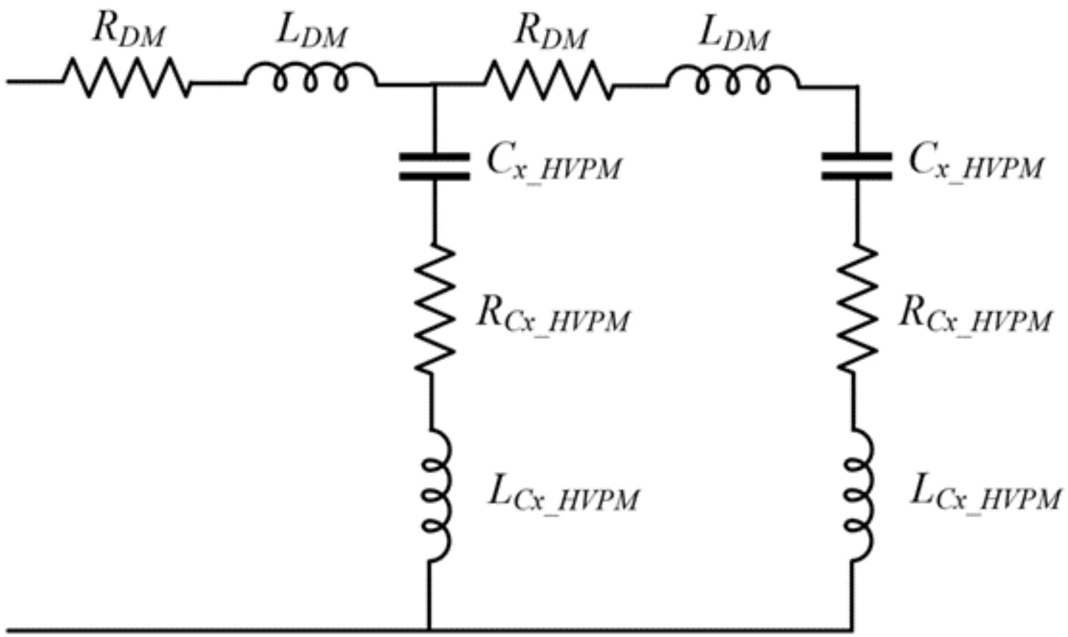


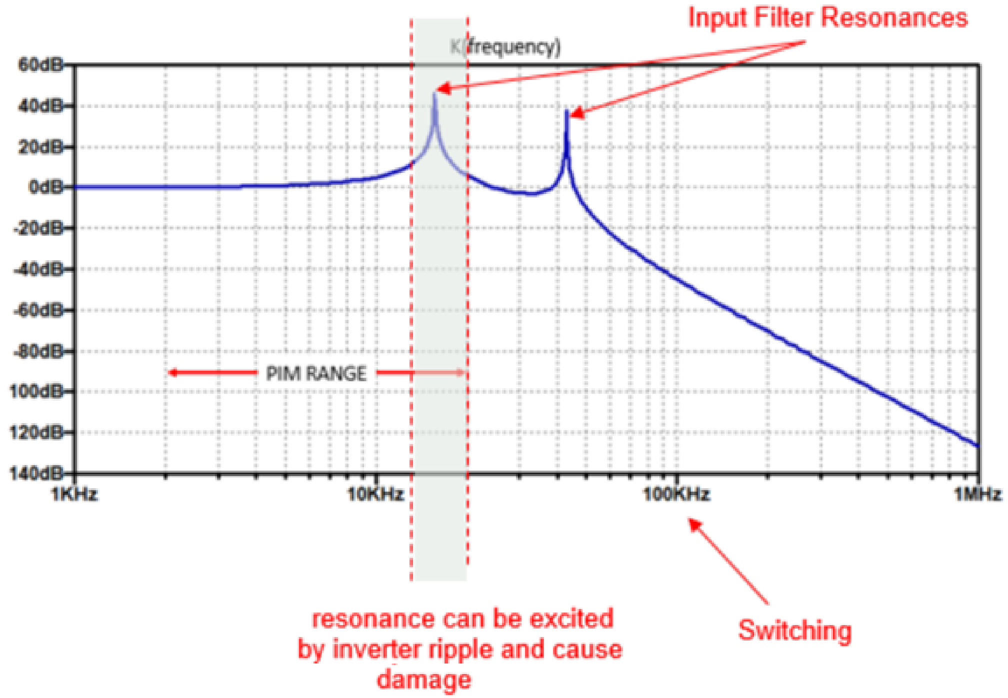
Impact of inverter ripple on DC-DC converter

- Component degradation:
  - DC-DC input filter capacitors are exposed to both DC-DC switching current and inverter ripple
  - Self-heating caused by $(I_{rms}^2 R_{ESR})$ leads to component degradation
- Ripple transfer to DC-DC output
  - DC-DC closed-loop bandwidth limited to a few kHz
  - Inverter ripple frequency not rejected by control loop
  - Ripple not filtered by input filter. Attenuated by transformer
  - Component damage (overvoltage) due to filter gain near resonance
  - Semiconductor devices must block (withstand) both HV_{DC} voltage AND ripple voltage superimposed onto HV_{DC} bus
  - Sufficient voltage breakdown margin required
- Filter resonances excited by inverter ripple will cause damage (over voltage and current)

Resonances: HVPM HVDC Filters

HV_{DC} filters are designed to address EMI noise and not inverter ripple.
If designed without taking inverter ripple into consideration, the filter can inadvertently be excited by inverter ripple



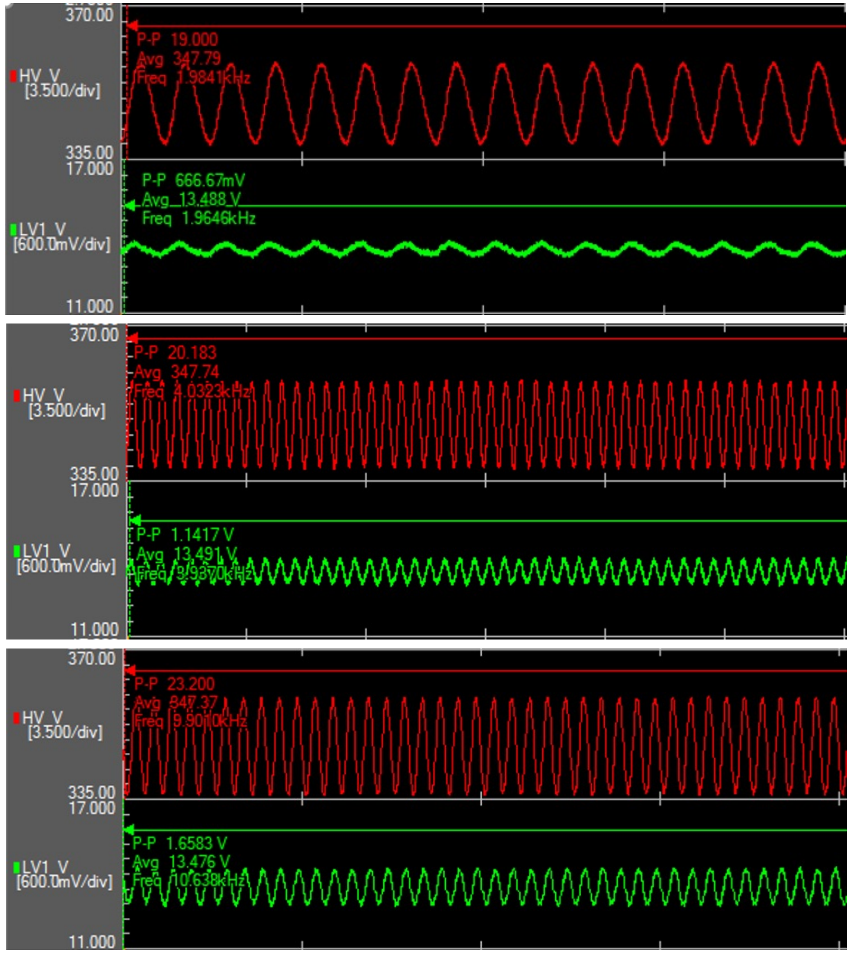


Ripple rejection – Example

HV Ripple:
Frequency = 2kHz
Magnitude = 19Vp-p
Converter Voltage Ripple
Magnitude: 0.7 Vp-p

HV Ripple:
Frequency = 4kHz
Magnitude = 20Vp-p
Converter Voltage Ripple
Magnitude: 1.14 Vp-p

HV Ripple:
Frequency = 10kHz
Magnitude = 23Vp-p
Converter Voltage Ripple
Magnitude: 1.7 Vp-p



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Solutions to address inverter ripple

- Minimize inverter ripple on HV bus:
  - Modify drive profiles
  - Increase DC link capacitance
  - Implement “No-fly” zones to avoid exciting component resonances
- Design converters which operate significantly higher above potential oscillations (ripple) on HV bus. The advantages are:
  - DC-DC converter at high switching frequency able to reject line ripple
  - Higher resonance for input filter means smaller filter size

High frequency, soft switching DC-DC and impact on EMI filter

- Increased power density
- Minimized voltage and current ripple
- Minimized EMI filtering effort
- Closed loop control bandwidth extended

Example/filter design: Design steps

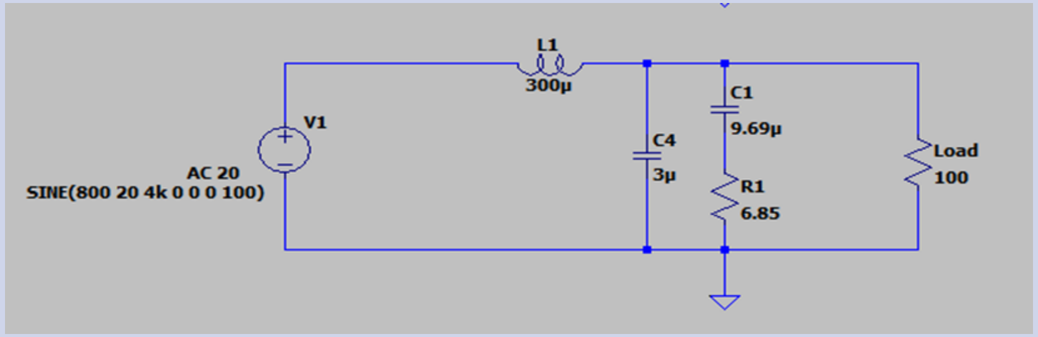
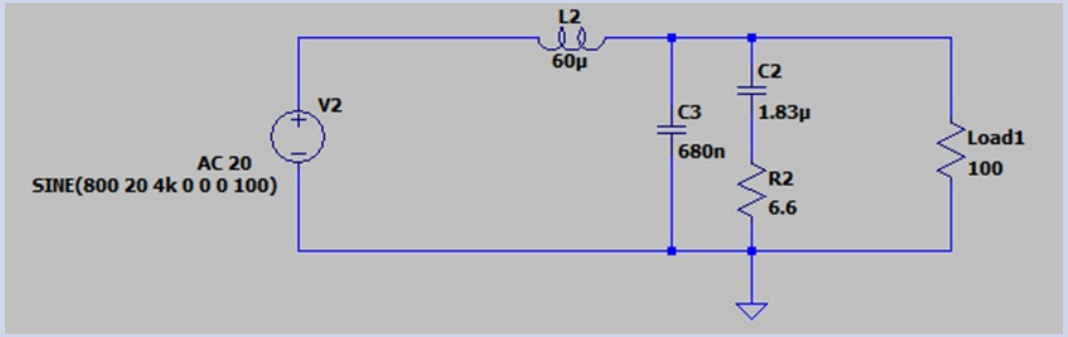
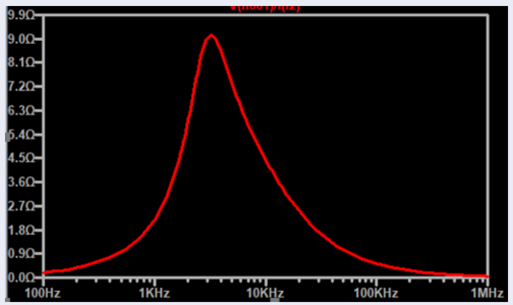
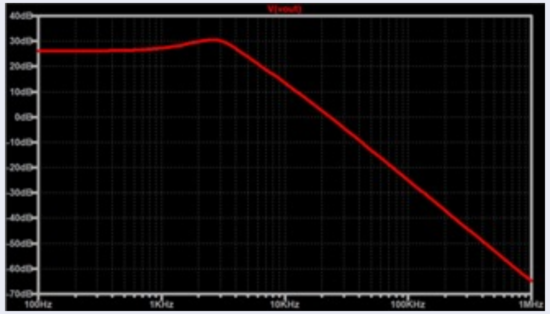
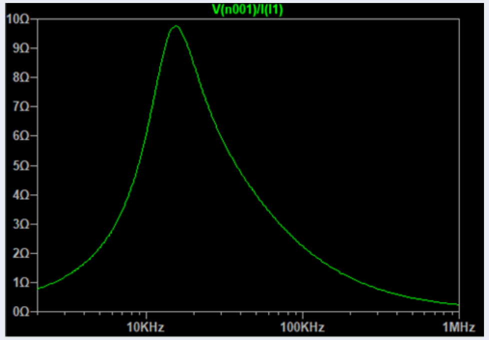
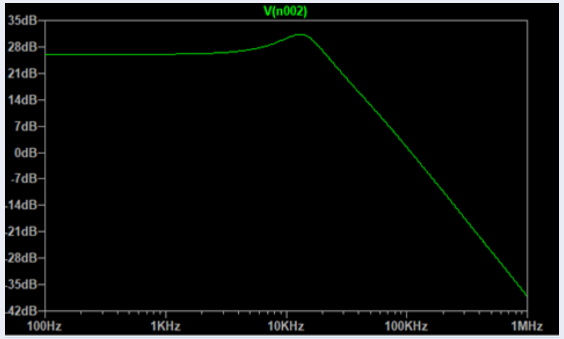
1. Select the cut-off frequency below the crossover frequency of the converter
2. Choose the inductor L based on maximum input current, calculate C based on equation or determine C based on voltage level and calculate L
3. Select appropriate filter network and calculate component values based on equations

(Middlebrooks theorem)

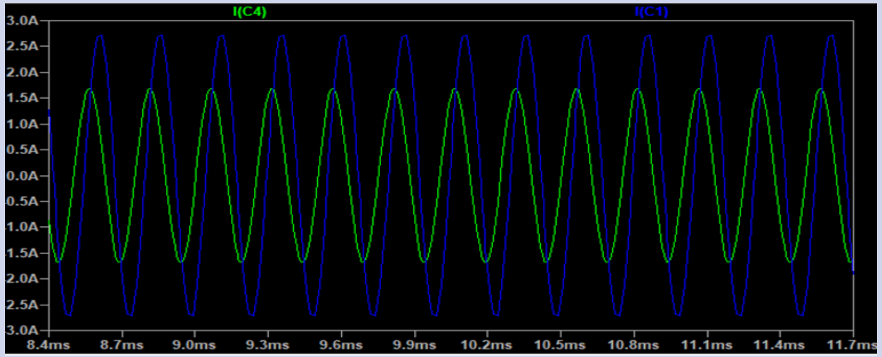
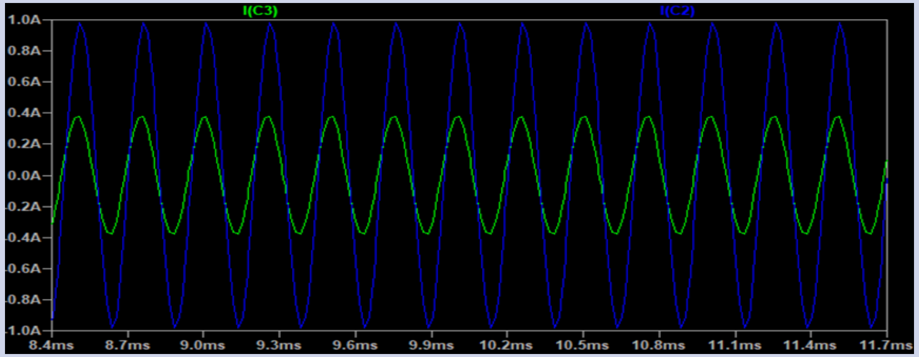
- Assume peak output impedance of the filter to be at least 10 times lower than input impedance of converter
- For 500V input and 2.5kW converter Z_{IN}=100Ohm

Apply these steps for two different DC-DC converters with 5kHz and 25kHz filter cut-off

Filter comparison

5kHz cut-off	25kHz cut-off
	
 	 

Filter Comparison – applying ripple voltage on HV input bus

5kHz cut-off	25kHz cut-off
	

Waveform: I(C4)

Interval Start:	8.4ms
Interval End:	11.7ms
Average:	22.049mA
RMS:	1.1904A

Waveform: I(C1)

Interval Start:	8.4ms
Interval End:	11.7ms
Average:	5.5372mA
RMS:	1.9315A

Waveform: I(C3)

Interval Start:	8.4ms
Interval End:	11.7ms
Average:	1.829mA
RMS:	264.69mA

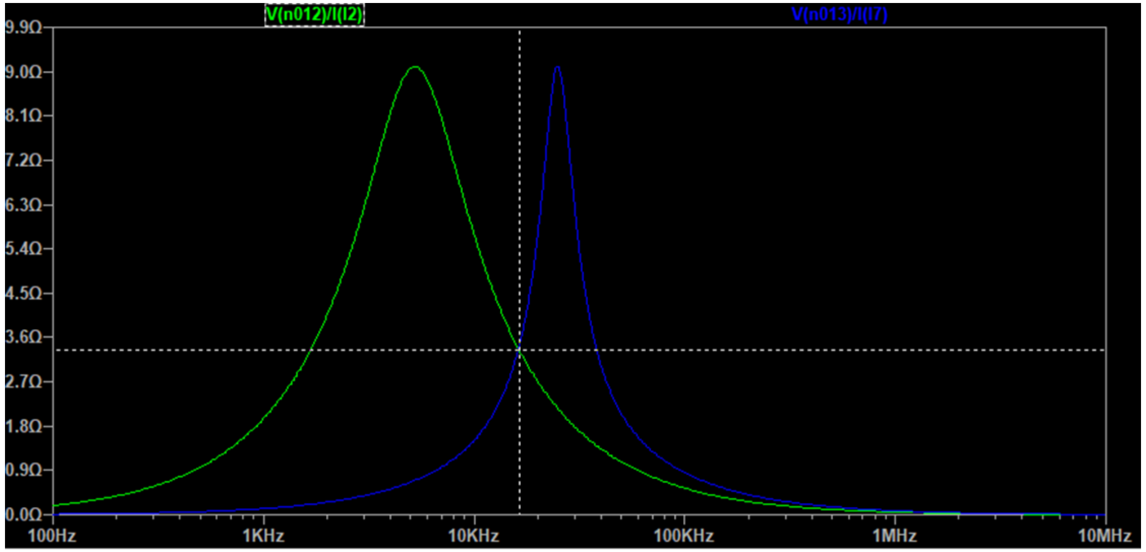
Waveform: I(C2)

Interval Start:	8.4ms
Interval End:	11.7ms
Average:	8.3599mA
RMS:	683.32mA

Filter output impedance

In order to keep filter losses lower, output impedance of the high cut-off filter should be below output impedance of the low cut-off, until frequency of interest

Lower impedance – lower losses, break even point 16kHz



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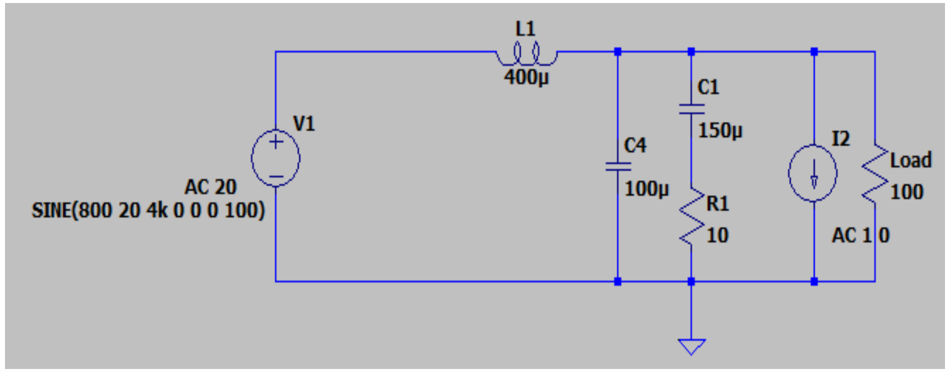
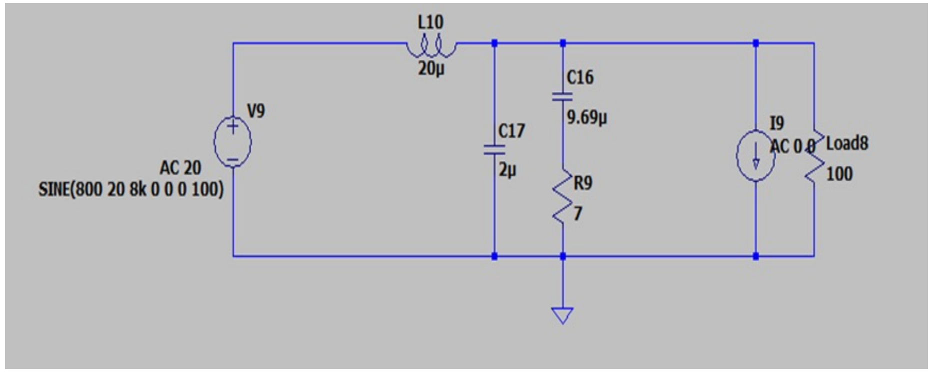
Size comparison – for filters with equal power losses

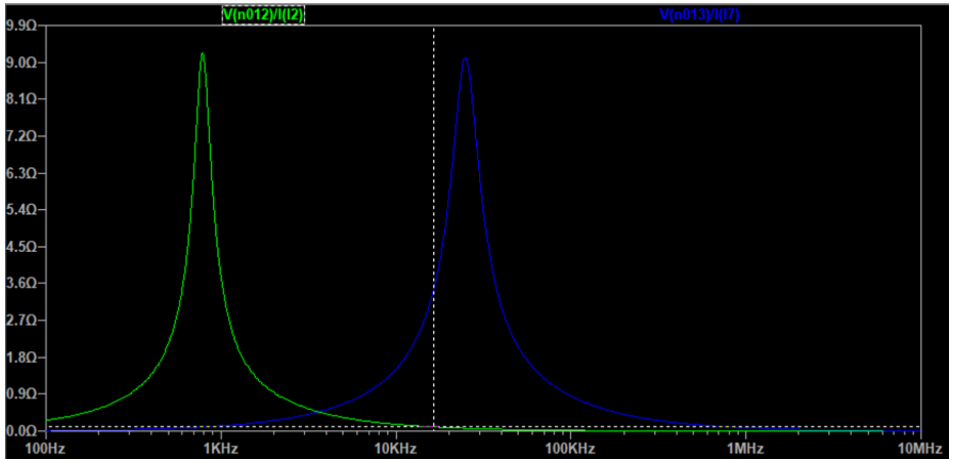




L1= 20 x L10
C4= 50 x C17

To keep losses equal and distributed

ONLY EXAMPLE



Filter topology influence

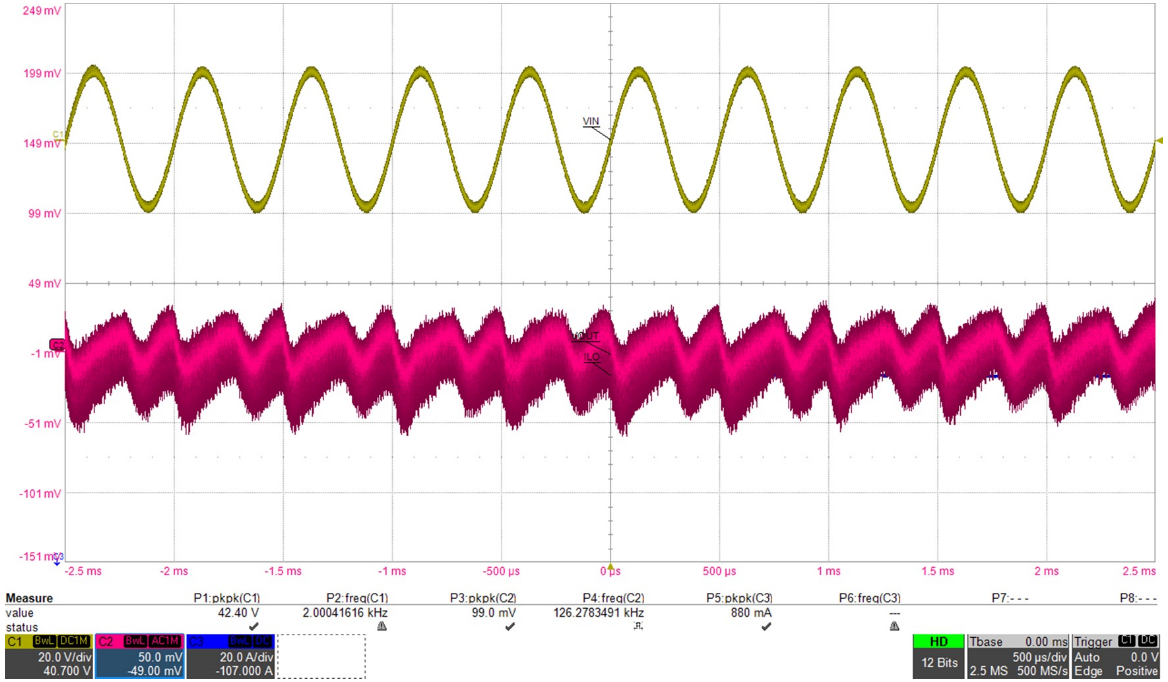
- Undamped filter
  - Risk of uncontrolled voltage amplification
  - Avoid inverter switching frequency
- Simplified damped
  - Weak attenuation at higher frequencies
- Series or parallel damped
  - Dissipate energy in damping circuit
  - Attenuate noise

Series damped might be more attractive due to lower current at high voltage level.

Relative size ratio will remain the same.

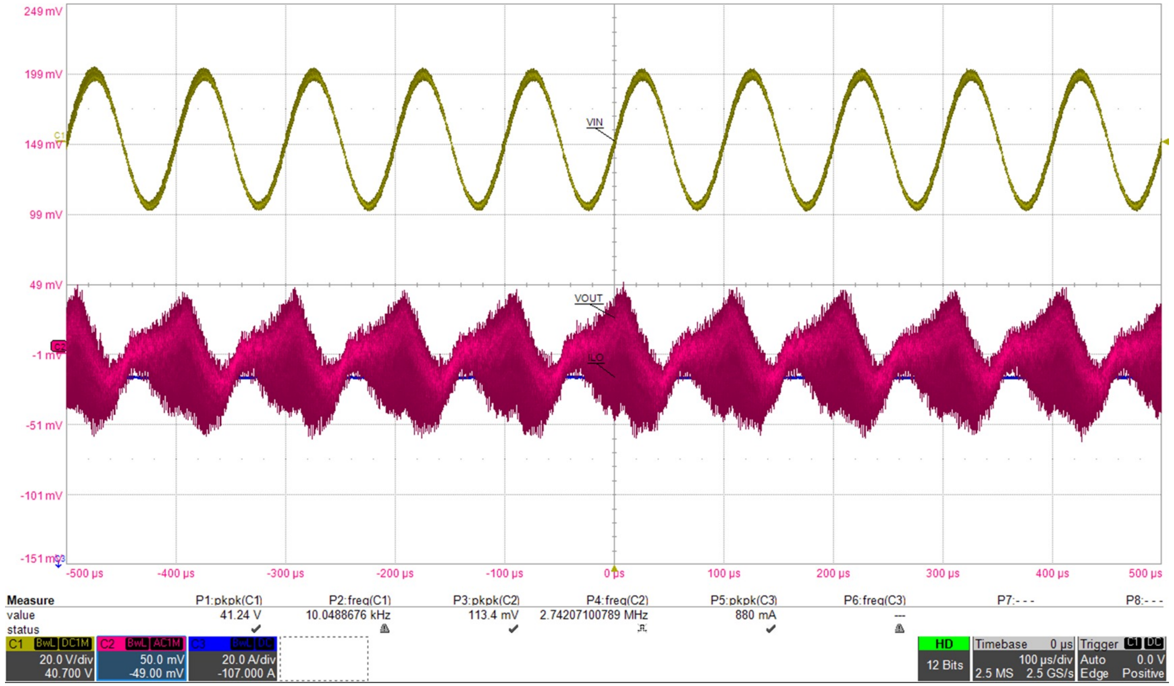
Vicor’s DC-DC converter under HV ripple – time domain

V_{IN} = 700 + 20*sin(2*pi*2k*t)



Vicor's DC-DC converter under HV ripple – time domain

$V_{IN} = 700 + 20*\sin(2*pi*10k*t)$



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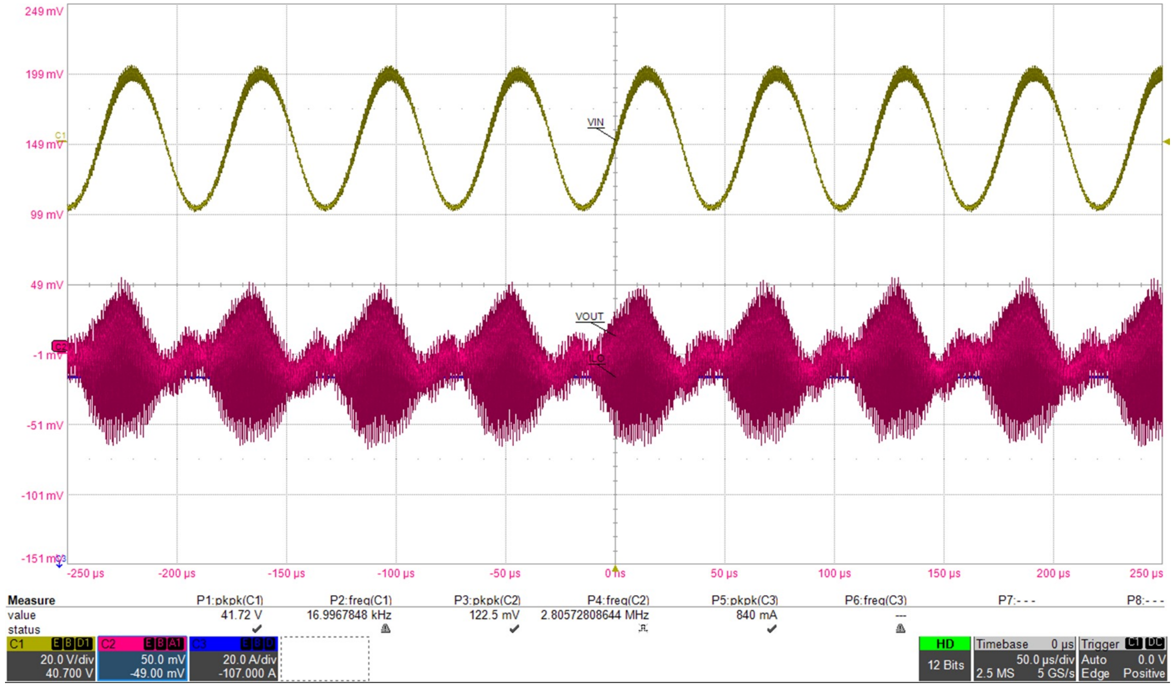
Vicor’s DC-DC converter under HV ripple – time domain

V_{IN} = 700 + 20*sin(2*pi*17k*t)



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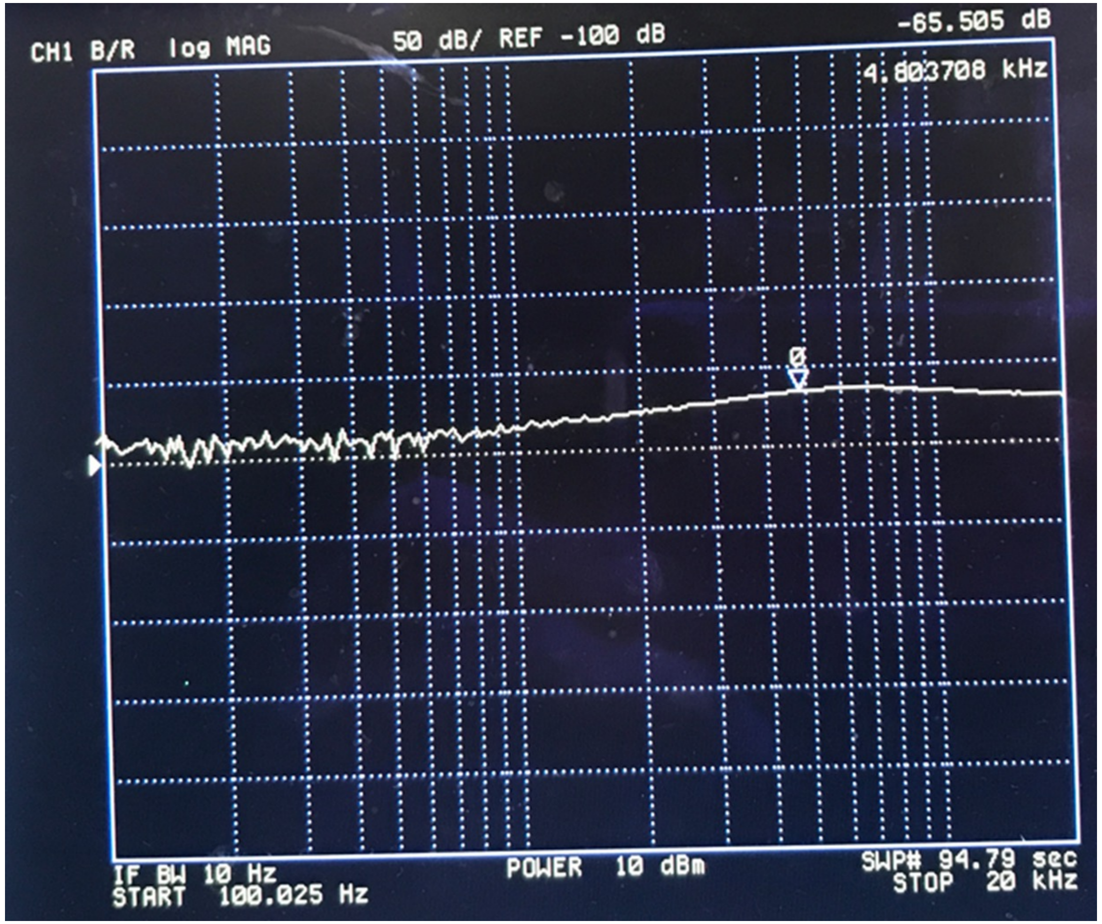
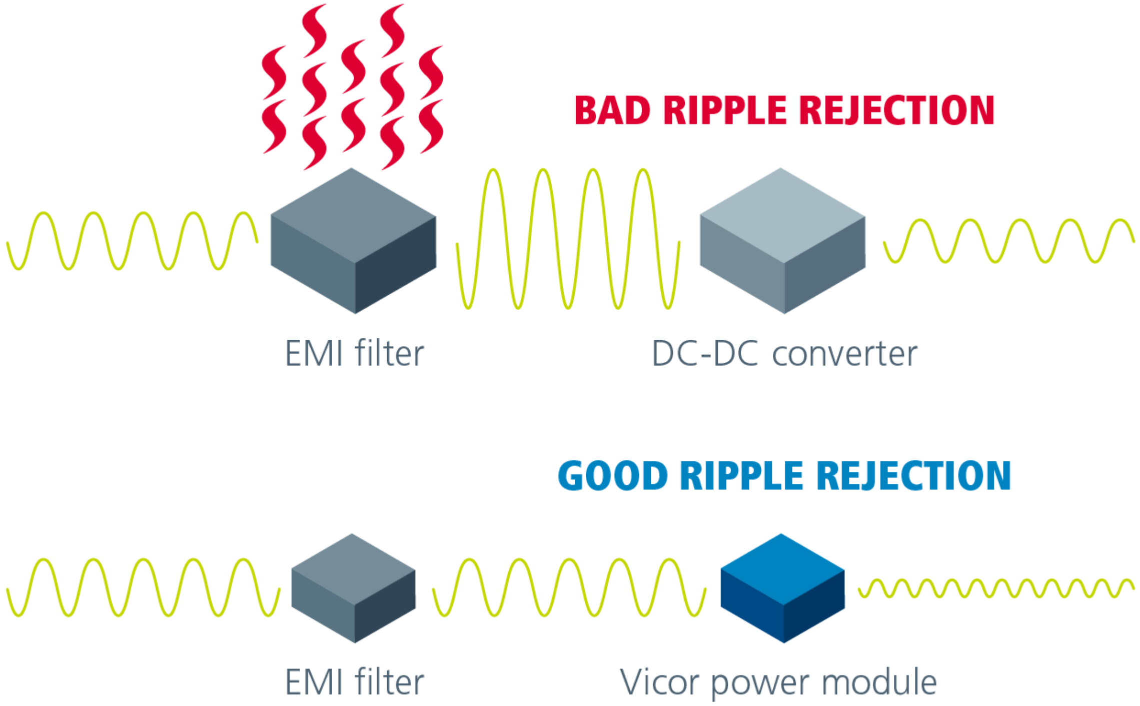
Vicor's DC-DC converter under HV ripple – frequency response



Conclusion

Vicor DC-DC converter enables:

- Highest power density conversion
- Smallest EMI filter (high switching frequency and ZVS/ZCS topology)
  - Shifting frequency range
- Reliable system and simplified architecture
- High frequency enable higher closed loop bandwidth and rejects inverter ripple noise



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Thank you

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